

FIG. 1

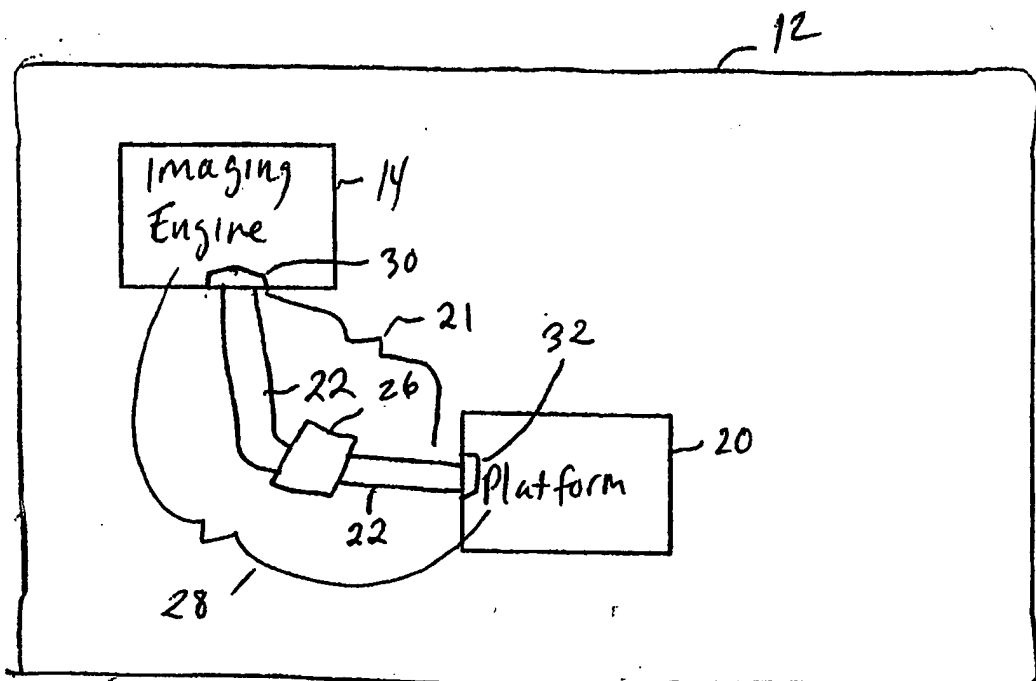


FIG. 2

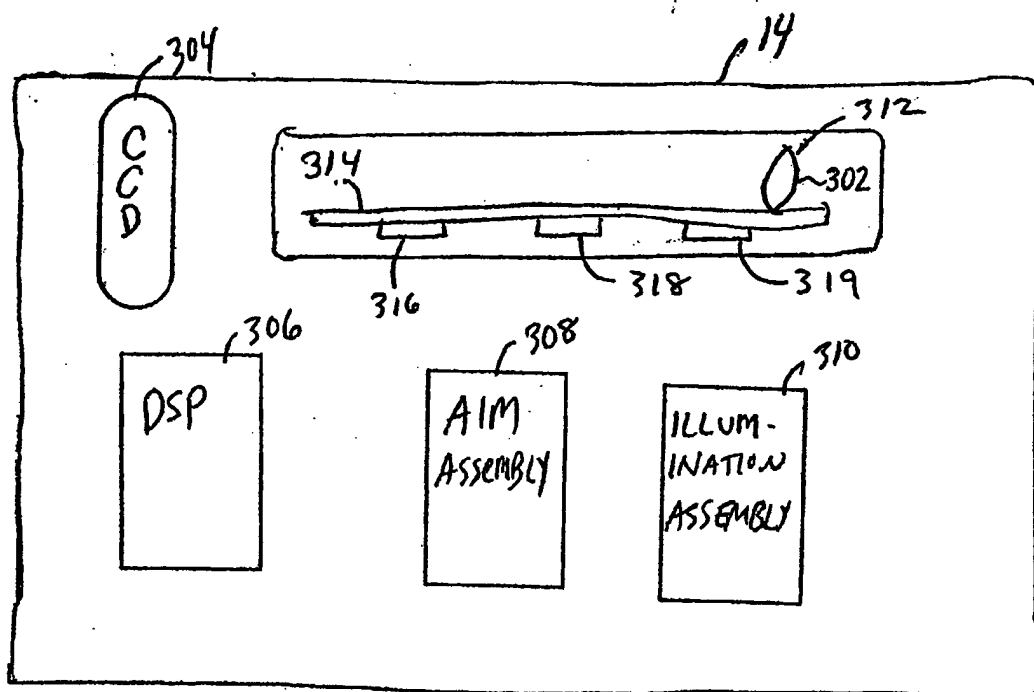
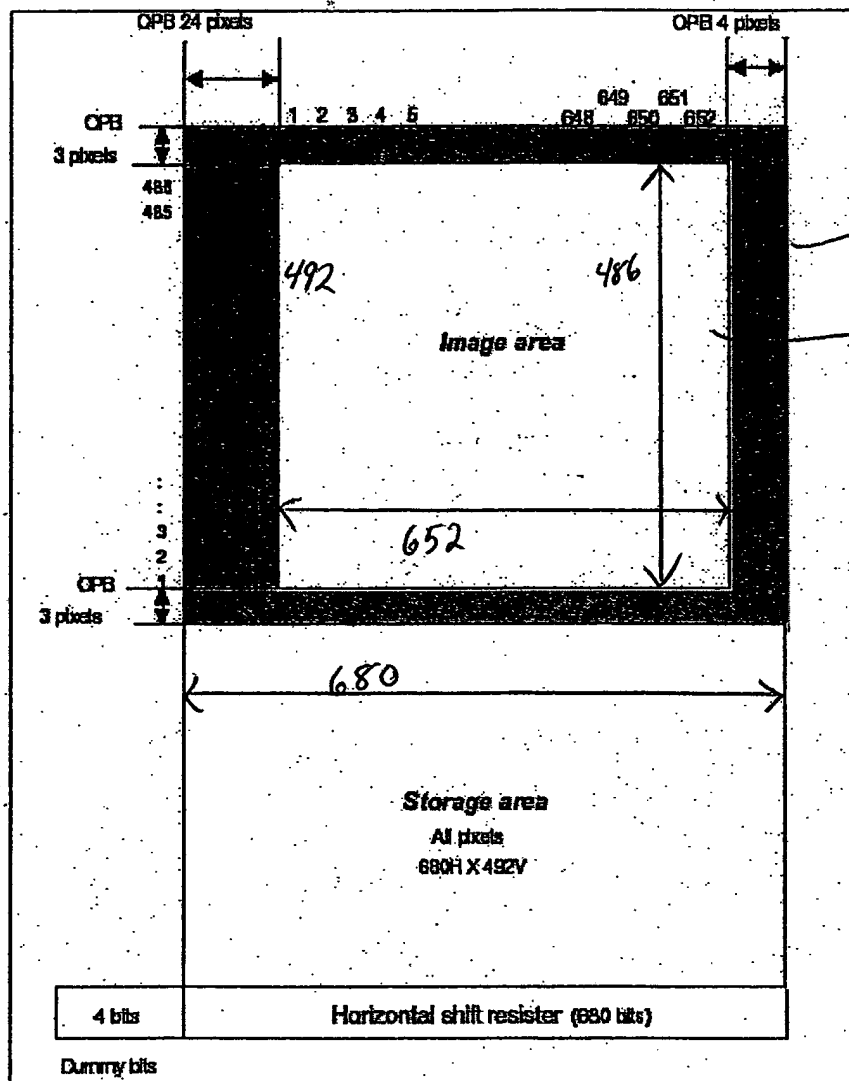


FIG. 3

PIn Number	Signal Name	I/O	Comments
1	GND	PWR	Ground
2	PCLK	O	Pixel Clock
3	GND	PWR	Ground
4	HREF	O	Horizontal Pixel Valid Clock (Sync)
5	VCC MOTOR	PWR	Focus Control Motor Power
6	VCC ILLUM	PWR	Illumination Power
7	REG RESET*	I/O	I2C Register Reset
8	VCC	PWR	CCD/Aiming Power
9	VCC	PWR	CCD/Aiming Power
10	EXSFT	I	External Frame Sync.
11	ILLUM ENB*	I	Illumination Enable
12	AIM ENB*	I	Aim Enable
13	PIX D0	O	Pixel Data Bit 0
14	PIX D1	O	Pixel Data Bit 1
15	PIX D2	O	Pixel Data Bit 2
16	PIX D3	O	Pixel Data Bit 3
17	PIX D4	O	Pixel Data Bit 4
18	PIX D5	O	Pixel Data Bit 5
19	PIX D6	O	Pixel Data Bit 6
20	PIX D7	O	Pixel Data Bit 7
21	FOCUS CTRL1	I	Focus Control Line 1
22	VREF	O	Vertical Frame Valid Clock (Sync)
23	EXHT	I	External Horizontal Clock
24	I2C_SDA	I/O	I2C Data
25	I2C_SCL	I	I2C Clock
26	GND	PWR	Ground
27	MCKI	I	Master Clock
28	GND	PWR	Ground
29	FOCUS CTRL2	I	Focus Control Line 2
30	CS*	I	Chip Select
31	FRAME SHIFT	O	Frame shift after exposure for Mode 1

Fig. 4



500

FIG. 5

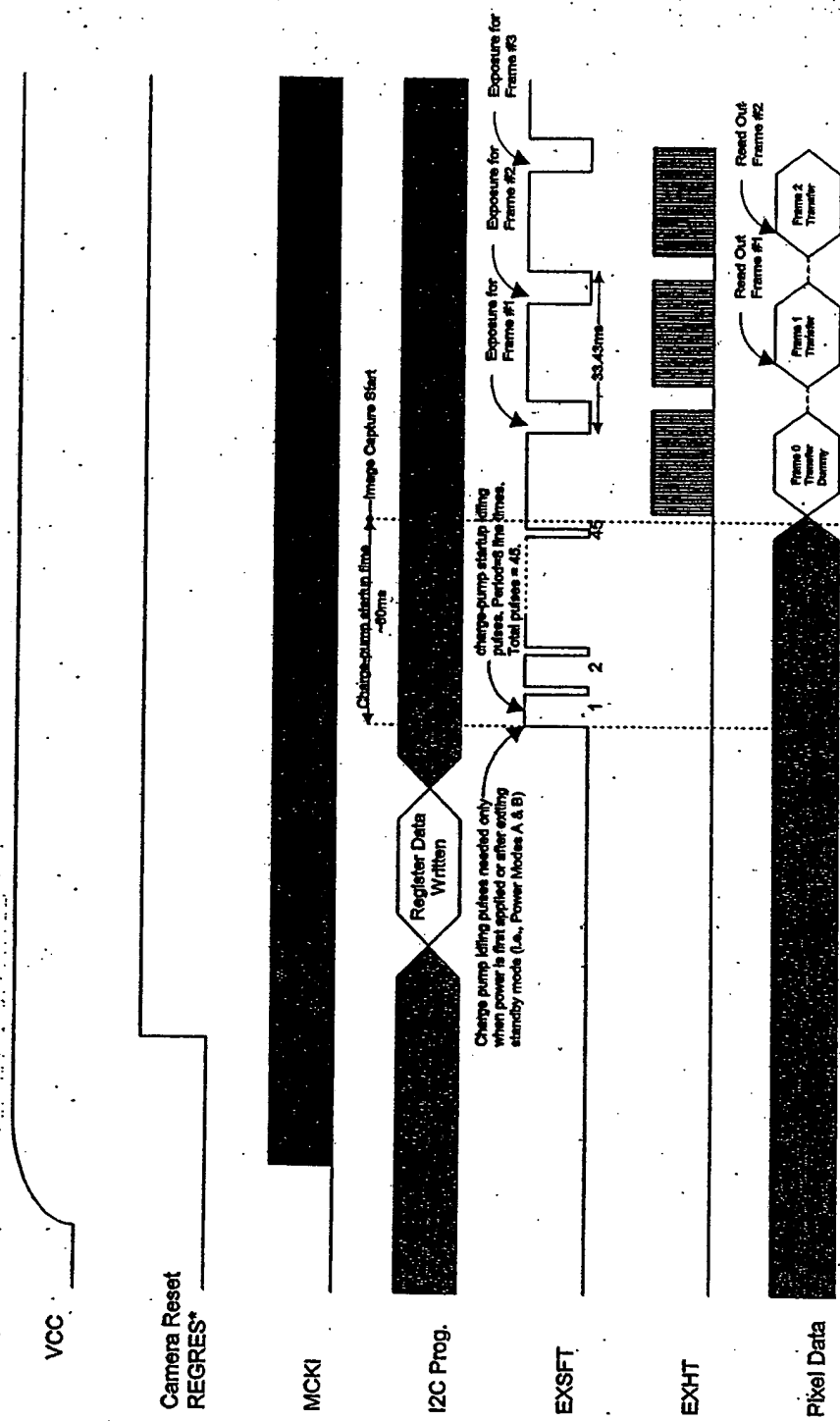


FIG. 6

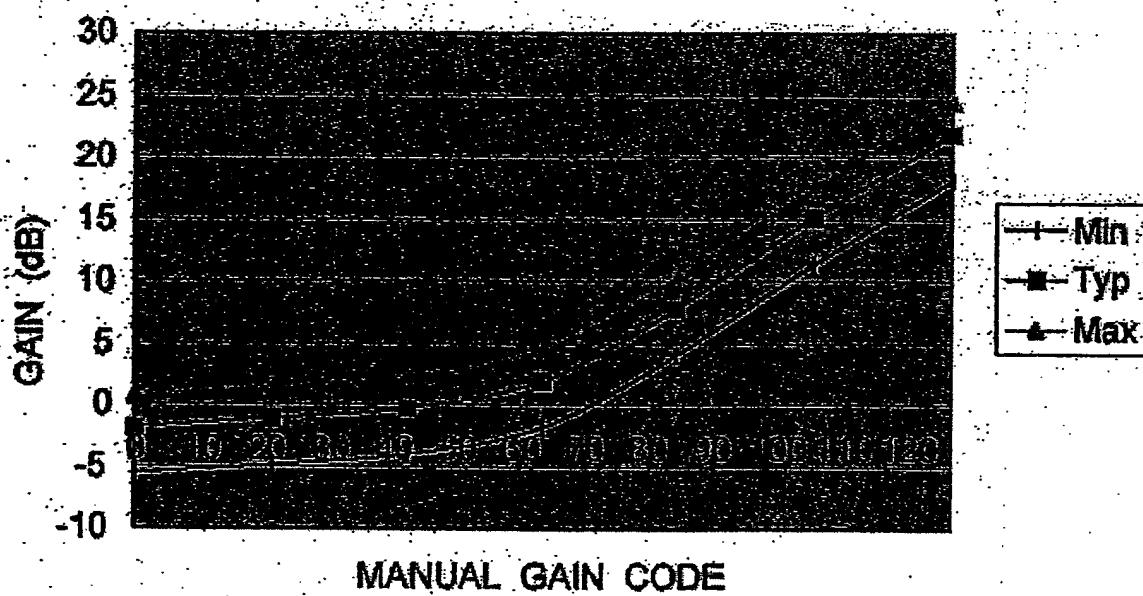


FIG. 7

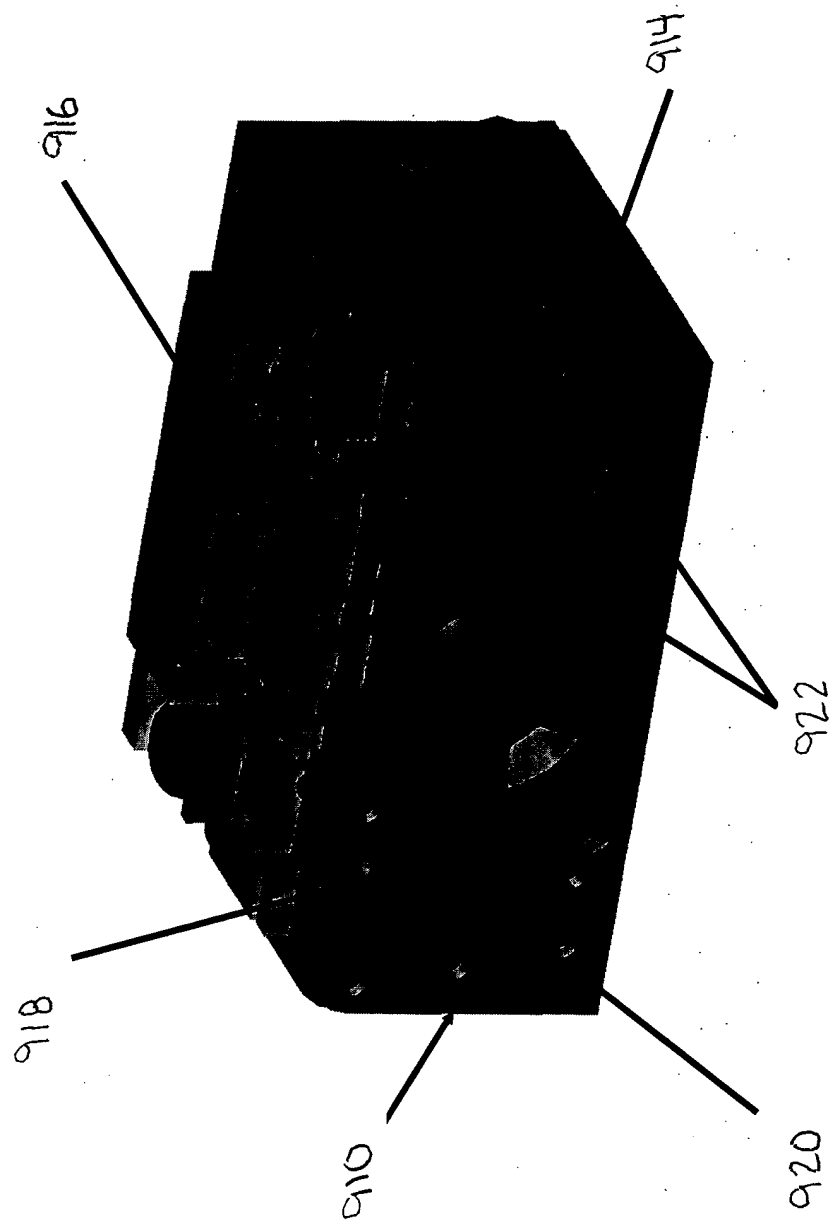


FIG. 8

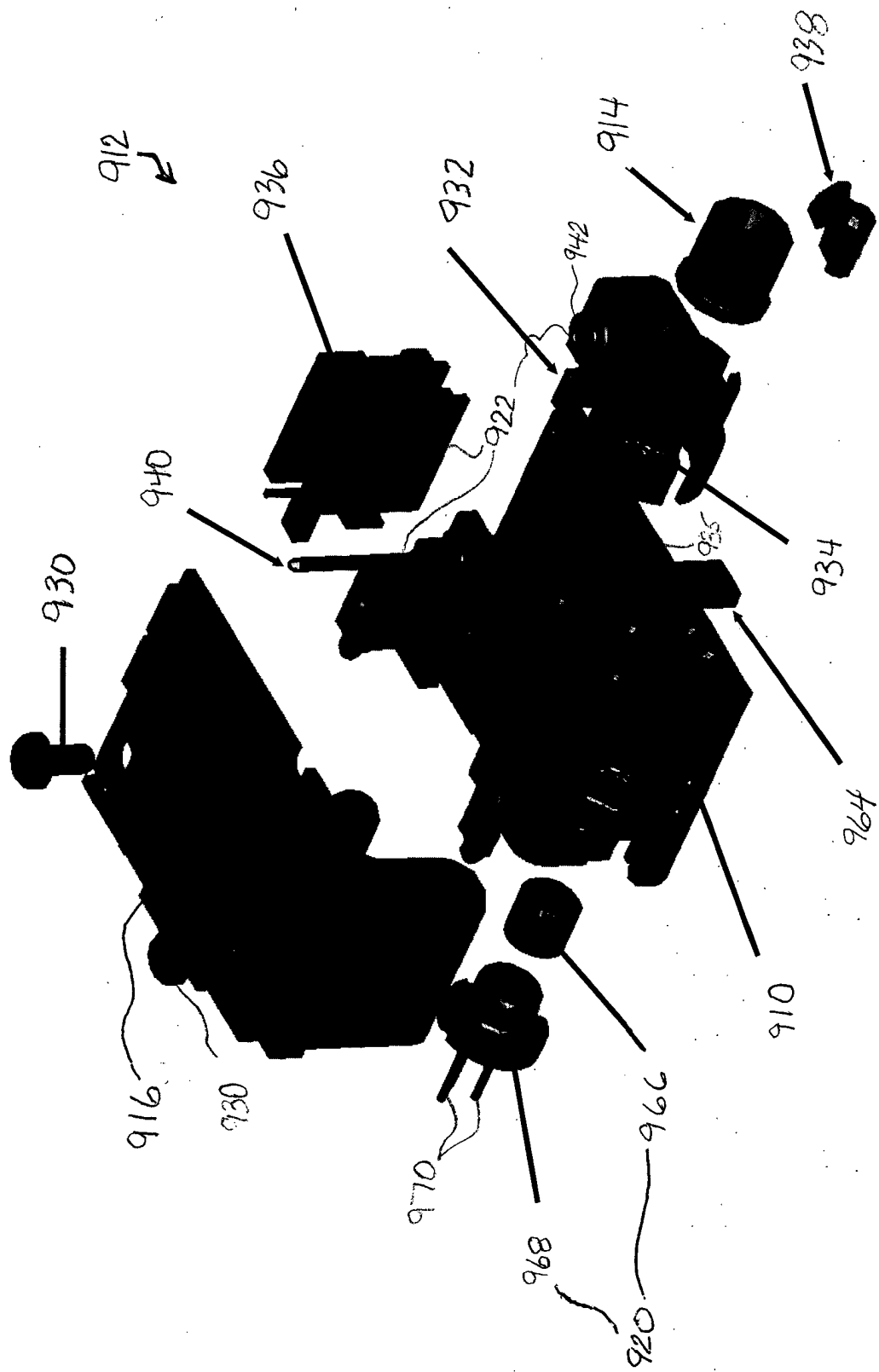


FIG. 9

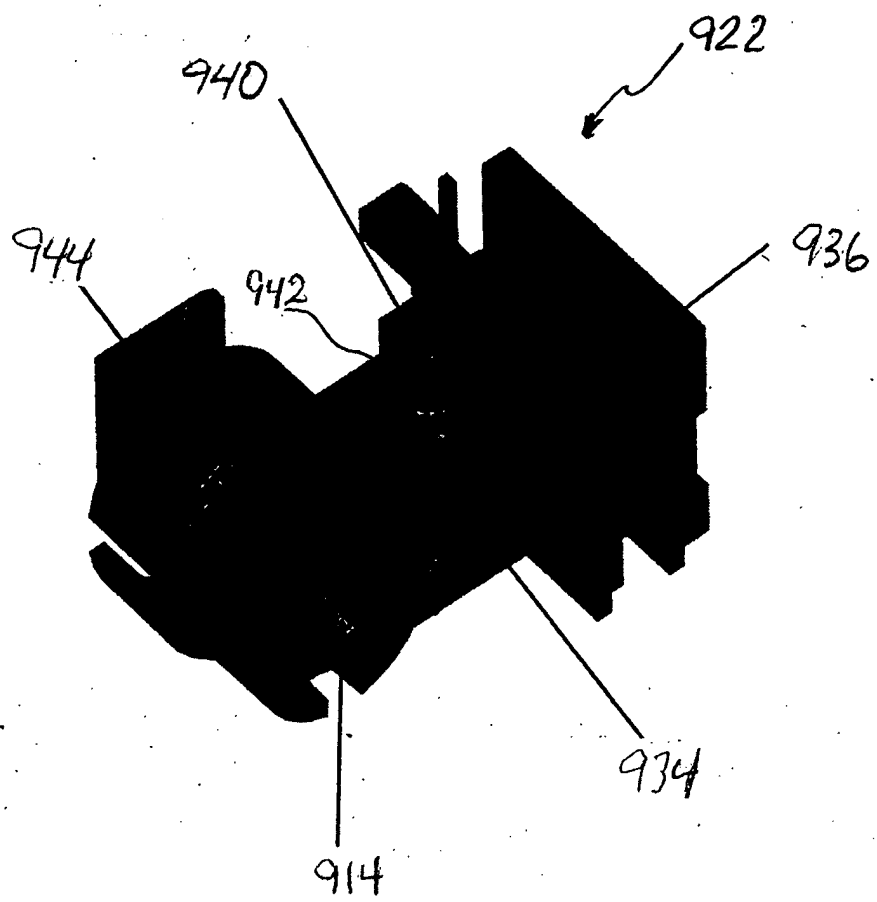
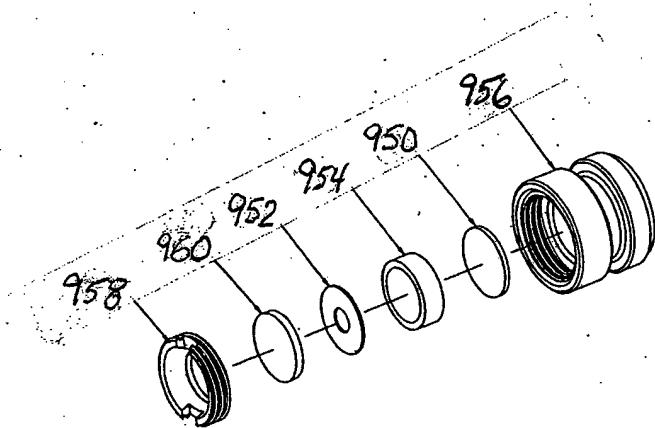


FIG. 10



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FIG. 11